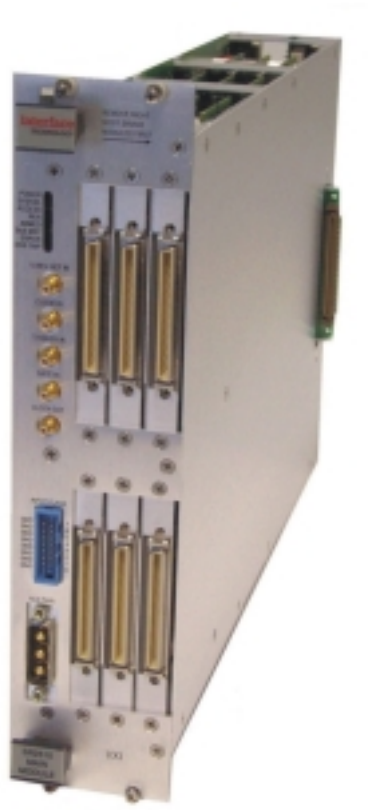
SR2500

Low Per-Pin Cost VXI Digital Test Subsystem



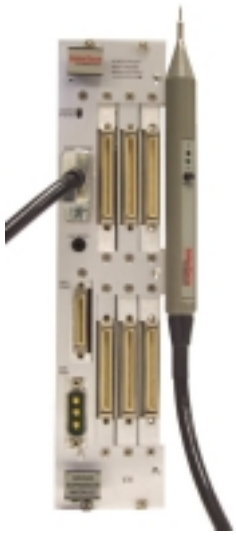
- DC to 25 MHz Data Rates
- 64K Vector Depth, 256K optional
- Stimulus / Response / Real Time Compare / Record
- 32, 64, or 96 Inputs and 32, 64, or 96 Outputs in a Dual-Slot VXI Module
- Expandable to 576 Inputs and 576 Outputs in a Single VXI Chassis
- Algorithmic and RAM-Backed Pattern Generation
- Multi-Level Triggering and Advanced Logic Analysis
- Data Formatting with Programmable Edge Placement
- A32 / D32 Binary Transfer for High-Speed Test Program Download
- Multiple Logic Families Supported Through Plug-In Modules
- Conditional Pattern Looping and Branching For Real Time Test Sequence Control
- Guided Probe Capability

25 MHz

SR2500 System Overview

The SR2500 is made for the test engineer on a tight budget who needs a high performance, high capacity, and cost effective solution to a wide range of demanding digital testing problems. It provides high-speed (25 MHz) digital pattern generation, response comparison, and logic analysis for both serial and parallel test requirements. A complete SR2500 subsystem comprises the SR2510 Main Module and up to five SR2520 Expansion Modules. The SR2510 is a dual-width VXI module that contains timing and control logic plus space for up to 96 inputs and 96 outputs. The SR2520 is also packaged in a dual-slot C-Size VXI module that provides up to 96 user selectable inputs and outputs. Modules can be configured at the time of order as bidirectional or unidirectional I/O channels. The number of input and output pins in the SR2510 and SR2520 modules are expandable internally in groups of 32 inputs and 32 outputs. Standard TTL, Differential ECL, Differential TTL, LVDS, 5 V CMOS, and 3.3 V logic families are supported in groups of 16 inputs and 16 outputs through the use of internal interface adapter boards. Variable voltage logic is supported in groups of 32 bidirectional channels.

WaveEdit Digital Waveform Editor, (optional).



SR2520 with Guided Probe Option.

Simple Test Program Development

The SR2500 is supplied with fully compliant VXI Plug & Play software drivers that includes a stand-alone, executable soft front panel program to interactively control the instrument. The soft panel provides complete control of the instrument without requiring a specific programming environment. A standard

installation program allows for quick setup and the ability to get up and running in minutes. This control software also includes standardized instrument drivers to control the instrument from within your application program. Both National Instruments LabView and LabWindows/CVI graphical programming languages are supported to provide interactive screens for micro-management of virtually any digital test application.

The SR2500 uses an ASCII message-based command set based on the SCPI-syntax (Standard Commands for Programmable Instruments) test language. The use of SCPI syntax simplifies test program development by providing an "English-like" programming environment that is widely accepted by the test and measurement industry.

Test program development is further simplified by data entry editing commands such as Pin Assignments. This allow you to group the I/O pins by their logical function (address bus, data bus, etc.) and assign a field name to that pin group. Pin Assignments streamline programming by allowing you to enter patterns by referring to the UUT signal names.

To simplify test development even easier, an optional graphical waveform editor (WaveEdit) can be added to the existing SR2500 WIN VXI Plug & Play Soft Panel. WaveEdit allows you to define stimulus and response test patterns using waveform graphics in order to represent data in the same familiar format that you use everyday. Recorded data can also be viewed in context with stimulus data permitting you to be more productive in developing and debugging test programs.

Fast Test Program Downloading From Slot-0 Controller

SR2500 test programs and stimulus / response test patterns may also be downloaded from the Slot-0 Controller using high-speed binary block transfers, thus providing the best of both worlds, i.e., ASCII based test language for simple test program development and binary block transfers for high speed download of test programs. To further minimize test download time, the SR2500 provides internal program storage capable of storing up to 128 different test programs. Any test program can be 'activated' by selecting its test name with a simple command string.

RAM-backed and Algorithmic Pattern Generation

The SR2500 offers traditional RAM-backed pattern generation and compare, while also providing algorithmic pattern generation and compare capabilities. Test patterns that would otherwise consume large amounts of I/O memory, such as for RAM memory testing, can be reduced to just a few algorithmic commands.

Algorithmic capability reduces the need for large pattern memory, increases test throughput by minimizing test download time, and reduces test programming and debug time.

Timing / Control Board

The SR2510 Timing and Control board, within the SR2510 module, provides clocking and test sequence control functions for all I/O boards within the SR2510 module and for any additional I/O boards contained in any SR2520 Expansion I/O modules used in the same SR2500 Digital Test Subsystem.

The SR2510 module has a dual processor architecture that is optimized for digital testing. The System Processor, the powerful 68030 running at 25 MHz, provides the VXI Bus message-based interface to the Slot-0 Controller. The Control Processor is the real-time digital test engine controlling the conditional test branching, looping, sequencing and logic analysis trigger evaluation.

VXI Bus Interface

Based on the IT9010M industry standard VXI bus interface chip, the SR2500 meets the requirements of VXI Bus Specification Versions 1.3 and 1.4. The SR2510 VXI bus interface receives message-based commands from the Slot-0 Controller, then becomes the VXI Bus Master to pass test parameters and data to the SR2510 internal I/O boards and to the SR2520 external I/O modules. The System Processor provides the command power for the SCPI-syntax word serial command structure.

Real Time Digital Testing

The 25 MHz Control Processor provides real time control of the test pattern sequence by controlling nested looping and conditional branching. This capability allows the SR2500 to generate stimulus patterns to the UUT, analyze the UUT response patterns, and determine the next test pattern based on test conditions such as expected response pass/fail, loop count, external input flags, response trigger qualifiers, etc.

Powerful Macro Commands Control Test Execution and Data Analysis

Stimulus pattern and response compare sequencing is controlled through a Test Program Macro Command language. The test program language contains over 100 macro command combinations to control the test sequence. All this digital testing capability is performed at full test speed and in real time, thereby, freeing your Slot-0 Controller from extensive response data analysis.

High Performance Response Logic Analysis.

The Record capability of the SR2500 is similar to that of an advanced logic analyzer. For simple logic analysis and recording, Trace Macro Commands allow you to quickly and easily program pre-trigger, center-trigger, and post-trigger conditions. The Advanced Trace Macro Commands provide a higher level of logic analysis performance by providing 16 Trigger Sequences. Each Trigger Sequence can trigger on any combination of up to 8 Response Qualifier Trigger Words. When trigger conditions are met, the trigger action can determine whether UUT response data or UUT compare error data will be recorded to memory.

Compact and Flexible Design

The SR2510 I/O boards are register-based companions to the message-based Timing / Control board. Each I/O board provides 32 I/O channels. The SR2510 can accommodate up to three I/O boards (up to 96 channels) and up to five SR2520s, each containing up to three I/O boards (96 channels), and all can be included in a single SR2500 Digital Test Subsystem. Thus, up to 18 I/O boards can be controlled by the Timing / Control board for a total of 576 bidirectional pins. Standard TTL, Differential ECL, Differential TTL, LVDS 5V CMOS, and 3.3 V logic families are supported in groups of 16 inputs and 16 outputs through the use of an internal interface adapter board. Variable Voltage logic from -3V to +7V is supported in groups of 32 bidirectional channels.

Seven Distinct I/O Memory Types

The SR2500 I/O board contains seven separate memory banks, each 64K vectors in depth (256K optional), for generating stimulus patterns, expected response patterns, and recording UUT response data. All memory banks operate at full 25 MHz data rates.

The Stimulus Memories consist of the Output, Tristate and Algorithmic Output memories. The Output Memory contains the actual data patterns to be supplied to the UUT. Tristate Memory provides tristate control which supports bidirectional I/O. The Algorithmic Output Memory determines which algorithmic pattern will be output.

The Response Memories consist of the Expect, Mask, and Algorithmic Expect memories. The Expect Memory contains the expected response data for the UUT and is the basis for input compare operations. The Mask Memory determines which patterns are to be ignored for input response comparison. Algorithmic Expect Memory determines which algorithmic expect pattern will be compared against the UUT input response.

Record Memory is used to store either the UUT response data or the result of the comparison between the UUT response data and the expected response pattern. It is operated independently in a manner much like a logic analyzer. A 16-level state machine and system-wide comparators are used to control which data is saved in the memory. In addition to the record memory, each input channel is provided with a 16-bit CRC register for signature analysis applications.

Data Formatting With Programmable Edge Placement

Stimulus pins may be independently programmed for any of the following data formats: Non-Return to Zero (NRZ), Return to Zero (RZ), Return to One (R1), Return to Complement (RC), and Return to Inhibit / Tristate (RI).

Formatting and Timing

Each SR2500 I/O board contains 6 high resolution timing generators for every 32 I/O channels, which are used to control stimulus edge placement and sample timing. Four of these timing generators are used with data formatting controls to provide delay and pulse width timing for the stimulus channels. The remaining two timing generator channels are used to define edge and/or window sample timing for all 32 input channels. Each group of 32 output channels share four timing generator channels and the four channels may be used to provide two delay times, to provide two delay time / pulse width combinations, or to provide one of each. The two sample timing generators may be used to provide two edge sample clocks or one compare window.

SR2500 SPECIFICATIONS*

I/O Characteristics:	Differential TTL I/O	TTL I/O	Differential ECL I/O	CMOS I/O	Variable Voltage I/O	+3.3V Logic I/O	LVDS I/O
Output Drivers							
Type	DS26F31M	74F125	100324	74AC125	-- n/s --	74LV125	DS90C031
High Voltage (Voh)	3.2V typ	3.4V typ	-1.025V -0.870V[1]	4.2V, 24 mA typ	-1.5V to +7.0V[4]	3.2V typ	1.41 V typ
Low Voltage (Vol)	0.32V typ	0.55V max	-1.830V -1.620V[1]	0.4V, 24 mA typ	-3.0V to + 4.5V[4]	0.3V	1.07 V typ
Sink Current	20 mA @ 0.5V	64 mA max	-- n/a --	+24 mA max	50 mA max[2]	32 mA max	-- n/a --
Source Current	20 mA @ 0.5 V	15 mA max	-- n/a --	-24 mA max	50 mA max[2]	-32 mA max	-- n/a --
Output Swing	-- n/a --	-- n/a --	-- n/a --	-- n/a --	0.0V to 11.0V p-p	-- n/a --	-- n/a --
Resolution	-- n/a --	-- n/a --	-- n/a --	-- n/a --	10 mV	-- n/a --	-- n/a --
Absolute Accuracy	-- n/a --	-- n/a --	-- n/a --	-- n/a --	100 mV	-- n/a --	-- n/a --
Abs. Max. Volt. (Hi-Z)	-- n/a --	-- n/a --	-- n/a --	-- n/a --	-3.0V to +7.0V	-- n/a --	-- n/a --
Output Impedance	-- n/a --	100 ohms	-- n/a --	100 ohms	50 ohms	100 ohms	-- n/a --
Input Receivers							
Type	DS26F32M	74ACT244	100325	74ACT244	-- n/s --	74ACT244	DS90C032
Diff. Input Volts (Vth)	0.2V min	-- n/a --	-- n/a --	-- n/a --	-- n/a --	-- n/a --	±200 mV min
Max Input Volts	±5.0V max	+5.0V max	-- n/a --	+5.0V max	-3.0V to +7.0V	+5.0V max	-0.3 to 4.8 V
Input Voltage, high (Vih)	-- n/a --	2.0V min	-1.165V -0.870V[3]	2.0V min	-- n/a --	2.0V min	-- n/a --
Input Voltage low, (Vil)	-- n/a --	0.8V max	-1.830V -1.475V[3]	0.8V max	-- n/a --	0.8V max	-- n/a --
Input Thrsh, high (Vth)	-- n/a --	-- n/a --	-- n/a --	-- n/a --	-2.9V to +5.5V	-- n/a --	-- n/a --
Input Thrsh, low (Vtl)	-- n/a --	-- n/a --	-- n/a --	-- n/a --	-2.9V to +5.5V	--- n/a --	-- n/a --
Resolution	-- n/a --	-- n/a --	-- n/a --	-- n/a --	10 mV	-- n/a --	-- n/a --
Absolute Accuracy	-- n/a --	-- n/a --	-- n/a --	-- n/a --	100 mV	-- n/a --	-- n/a --
Input Impedance	100 ohms	10k ohms	50 ohms to -2.0V	10k ohms	> 50k ohms	10k ohms	100 ohms

Notes: n/a = not applicable; n/s = not specified; Note 1: Min-Max, Measured with 50 ohm termination to -2.0 V dc bus;
Note 2: Aggregate static source/sink current is 800 mA per 32 channels; Note 3: min-max, single-ended; Note 4: unterminated

CPU:
- System Processor: Motorola 68EC030 @ 25 MHz
- Control Processor: 25 MHz Custom Gate Array

Internal Clock:
- Range: 5.0 ms to 40 ns, 200 Hz to 25 MHz
- Resolution: ≤ 0.005%
- Data Output Jitter: 10 MHz reference jitter + 100 ps (short term RMS)

External Clock:
- Range: DC to 25 MHz
- Pulse Width: 20 ns (minimum)
- Active Edge: Rising or falling
- Input Voltage: -5.0 to + 10.0 V
- Input Threshold: -5.0 to +4.99 V, in 20 mV steps
- Input Impedance: 1 Megohm

External 10 MHz Ref Input:
- Input Coupling: Capacitor coupled
- Input Signal Waveform: Square to sine wave
- Input Voltage Level: 1-5 V p-p
- Input Impedance: High impedance

External Trigger Input:
- Active Edge: High or low
- Input Voltage: -5.0 to + 10.0 V
- Input Threshold: -5.0 to +4.99 V, in 20 mV steps
- Input Impedance: 1 Megohm

External Gate Input:
- Active Edge: Rising or falling
- Input Voltage: -5.0 to + 10.0 V
- Input Threshold: -5.0 to +4.99 V, in 20 mV steps
- Input Impedance: 1 Megohm

External Input Flags:
- Receiver Type: 74ACT244
- Number: Eight
- Active Level: High or Low
- Input Voltage: Vil < 0.8V; Vih > 2.0 V
- Input Impedance: 10k ohms

Clock Output:
- Driver Type: 74F244
- Output Level: TTL
- Pulse Width: 20 ns, minimum
- Output Termination: 50 ohm, series

I/O Timing:
- Delay Range: 1 Test Cycle
- Delay Resolution: 5-10 ns, depending on frequency
- Stimulus Format Clocks
  - Resolution: 5-10 ns, depending on frequency
  - Min. Pulse Width: 10 ns
  - Max. Pulse Width: 1 Test Cycle - 10 ns
- Response Sample Clocks (Edge or Window)
  - Resolution: 5-10 ns, depending on frequency
  - Min. Window Width: 10 ns
  - Max. Window Width: 1 Test Cycle - 10 ns
- Setup Time: 10.0 ns, min.
- Hold Time: 10.0 ns, min.
- Skew: ± 2 ns (typ) across same type I/O, within single module
  3 ± 1 ns (typ), across same type I/O, cumulative, across multiple modules

Data Formats:
- NRZ: Non-Return-to-Zero
- RZ: Return to Zero
- RONE: Return-to-One
- RC: Return-to-Complement
- RI: Return-to-Inhibit / Tristate

VXI Specifications

Interface Compatibility:
- SR2510: Message-based, Bus Master/Servant
- SR2520: Register-based, Servant
- Revision: 1.4
- Size: C-size, Dual slot
- Configuration: Static
- Interrupt Level: Programmable 1-7
- Triggers: TTLTRG 0-7
- Memory(SR2510): 1 MB VME A32/D32/D16/D8 (EO)

Power Requirements: (Note 2)
- +5.0 volts: 21.5 A, max.
- -5.2 volts: 1.0 A, max.
- +12.0 volts: 0.1 A, max.
- -12.0 volts: 0.1 A, max.
- -2.0 volts: 1.0 A, max.

Note 2: Power values specified are with three TTL I/O cards installed.

Cooling Requirements:
- Per Slot Avg.: 117 W, maximum per module (Note 2)
- Airflow: 8 liters / sec per module; 4 liters / sec per slot @ 0.2 mm of water pressure / 10°C temp. rise

Environmental Specifications:
- Temperature: Storage = -40°C to +75°C
  Operating = 0°C to +45°C
- Humidity: 5% to 95% relative, noncondensing

Software Drivers:
- National Instruments: LabView
- National Instruments: LabWindows/CVI

* *Specifications subject to change without notice.*

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